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SGS-THOMSON MICROEL *EP -430-403-A
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Semiconductor device inter-level contacts formation - by depositing refractory metal-contg. layer in contact hole followed by aluminium at elevated temp. for inter-facial alloying
C91-071793 R(DE FR GB IT)

Interlevel contacts in an IC device are formed by:
(i) forming a contact opening in an insulating layer to expose a conducting region;
(ii) depositing a refractory metal contg. conductive material on the layer and in the opening; and
(iii) depositing Al at a temp. of at least 150°C, (350-500 °C), to form an alloy of Al and the refractory metal in the opening.

ADVANTAGE

Method is simple and effective and is used for geometries of less than 1 micron.

PREFERRED METHOD

The Al is deposited at a rate of 20-200 Angstrom/sec. The vol. of alloy formed in the opening has a vol greater than that of the unalloyed Al and refractory metal.

L(4-C10C, 4-C13B)

The refractory metal-contg. layer is pref. a cpd; in an embodiment, a refractory metal is deposited, formed into a cpd, pref. nitride or silicide, and a second layer of refractory metal added.

PRODUCT

Semiconductor structure compriscs an insulating layer overlying a conductive region; an opening in the insulating layer; a refractory metal-contg. layer over the insulating layer and covering the sidewalls of the opening and the exposed conductive region; a layer of an alloy of the refractory metal layer and Al; and a top layer of Al. The refractory metal-contg. layer is pref. refractory metal nitride or silicide overlaid with a layer of refractory metal. (7pp1110HPDwgNo3/6).
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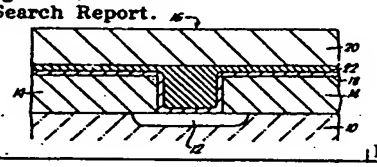

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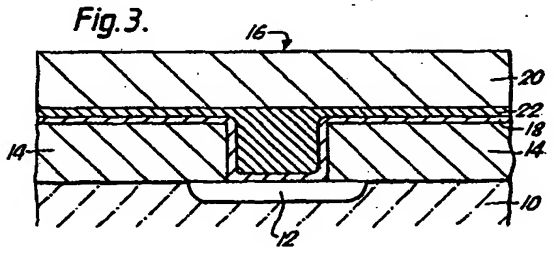
(54) Method for fabricating interlevel contacts.

(57) A method for fabricating interlevel contacts in semiconductor integrated circuits provides for formation of a contact opening through an insulating layer. A layer of refractory metal, or refractory metal alloy, is deposited over the surface of the integrated circuit chip. An aluminum layer is then deposited at a significantly elevated temperature, so that an aluminum/refractory metal alloy is formed at the interface between the aluminum layer and the refractory metal layer. Formation of such an alloy causes an expansion of the metal within the contact opening, thereby filling the contact opening and providing a smooth upper contour to the deposited aluminum layer.

Fig.3.



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METHOD FOR FABRICATING INTERLEVEL CONTACTS

The present invention relates generally to integrated circuit fabrication, and more specifically to a method for fabricating interlevel contacts.

Aluminum is used extensively in the field of semiconductor integrated circuit fabrication for providing interconnect between various portions of an integrated circuit chip. Aluminum has several important advantages which make it the conductor of choice for many applications. Among the properties which make aluminum so useful is the fact that it is very conductive, it forms a good mechanical bond with various dielectric layers generally used in a semiconductor industry, and it makes a good ohmic contact with both N and P type semiconductors.

Aluminum also has several important drawbacks which must be overcome when fabricating integrated circuits. Aluminum forms fairly low temperature alloys. As a result, its rate of self-diffusion can be significant at temperatures which fall within the expected operating range of the semiconductor circuits in which it is included. This movement of aluminum atoms is especially severe if the aluminum interconnect carries relatively high current densities. This phenomenon is known as "electromigration," and can cause premature failure of semiconductor devices. To prevent failures due to electromigration, semiconductors must be designed so that the current density in aluminum lines does not become enough to cause rapid electromigration.

Electromigration problems can become especially severe when aluminum interconnect lines cross abrupt height changes on the surface an integrated circuit. Such abrupt changes are generally referred to as steps. Thinning of aluminum interconnect lines tends to occur over such steps, increasing current density at these locations and making the device more susceptible to electromigration problems.

Step coverage problems are common when small openings are made through a relatively thick dielectric layer to allow contact with conductive regions beneath. These problems are especially severe with sub-micron device geometries. Contact openings, also referred to as vias, can be made to contact an underlying active region within a semiconductor substrate, or to contact an underlying polycrystalline silicon or metal interconnect layer. The sputter deposition or evaporation techniques used to form aluminum thin film layers produces a much thinner layer of metal along the edges of such an aperture due to a self-shadowing phenomenon. Th higher current densities found in the thinner sidewalls can contribute to significant electromigration problems for an integrated circuit device.

Present techniques for minimizing step coverage problems through small apertures includ creating apertures having sloped sidewalls and filling the contact opening with a refractory metal alloy. Creating sloped sidewalls on the contact openings increases their overall size, which limits device density. This is especially important for submicron devices. Filling the contact opening with a refractory metal alloy adds significant complexity to present process flows. Both of these techniques also tend to result in an uneven upper surface, making it difficult to stack contacts one abov another.

Another proposed technique for filling contact openings is to deposit a thin layer of aluminum at a low temperature, substantially room temperature, followed by deposition of a thick aluminum layer at 400° C or higher. Such an approach is believed to be difficult to perform, and results in contact openings which are still not completely filled. A thick aluminum layer must be used, and spiking problems can occur.

It would be desirable for a technique for manufacturing integrated circuits to provide for completely filling contact openings with a conductive material. It would be further desirable for such a technique to be simple and compatible with current processing technology.

It is therefore an object of the present invention to provide a semiconductor integrated circuit manufacturing method which causes contact openings to be completely filled with a conductive material.

It is a further object of the present invention to provide such a method which is suitable for use at geometries of less than one micron.

It is another object of the present invention to provide such a method which adds a minimal amount of complexity to current semiconductor processing techniques.

It is yet another object of the present invention to provide such a method which can easily b incorporated into existing integrated circuit process flows.

Therefore, according to the present invention, a method for fabricating interlevel contacts in semiconductor integrated circuits provides for formation of a contact opening through an insulating layer. A layer containing a refractory metal, or a refractory metal alloy, is deposited over th surface of th integrated circuit chip. An aluminum layer is then deposited at a significantly elevated temperature, so that an aluminum/refractory metal alloy is formed at the interface between the aluminum layer

and the refractory metal layer. Formation of such an alloy causes an expansion of the metal within the contact opening, thereby helping to fill the contact opening and providing a smooth upper contour to the deposited aluminum layer.

The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself however, as well as a preferred mode of use, further objects and advantages thereof, will best be understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings, wherein:

Figures 1 through 3 illustrate a preferred method for fabricating an interlevel contact according to the present invention;

Figures 4 and 5 illustrate an alternative method for forming an interlevel contact according to the present invention; and

Figure 6 is a cross-section of a portion of an integrated circuit illustrating formation of a second contact through an opening in a dielectric layer immediately above a first interlevel contact.

The process steps and structures described below do not form a complete process flow for manufacturing integrated circuits. The present invention can be practiced in conjunction with integrated circuit fabrication techniques currently used in the art, and only so much of the commonly practiced process steps are included as are necessary for an understanding of the present invention. Figures 1-6 represent a cross-section of a portion of an integrated circuit during fabrication. The figures are not drawn to scale, but instead are drawn so as to illustrate the important features of the invention.

Referring to Figure 1, a substrate 10 includes an active region 12 such as a source/drain region of a field effect transistor. A dielectric layer 14, such as silicon dioxide (SiO_2) is formed over the surface of the substrate 10. An opening 16 is formed in the dielectric layer 14 in order to allow an upper level conductor to make contact with the active region 12.

Referring to Figure 2, a thin layer of refractory metal 18 is deposited over the surface of the integrated circuit. This layer 18 can have a thickness varying from approximately 100 angstroms to more than 3,000 angstroms. The layer may consist of a refractory metal such as titanium, molybdenum, or niobium. Alternatively, an alloy or compound containing a refractory metal, such as titanium/tungsten, titanium nitride, or molybdenum silicide.

Referring to Figure 3, a layer of aluminum 20 is then deposited over the surface of th chip. This layer is d posited at an elevated temperature of at least approximately 150°C. A higher deposition rate of aluminum can be used at high r temperatures, so the aluminum layer 20 is preferably deposited at a temperature between approximately 350°C and 500°C preferably at a rate of approxdmately 20-200 A/sec. In addition, the higher deposition temperatures increase the surface mobility of the deposited aluminum, increasing the amount of aluminum deposited in the contact opening 16.

Depositing the aluminum layer 20 at such an elevated temperature causes it to alloy with th refractory metal layer 18 to form an aluminum/refractory metal alloy layer 22. The volume of the aluminum/refractory metal alloy is greater than the volume of the aluminum and refractory metal separately, so that voids within the contact opening 16 are filled by the expanding alloy. The area of the interface between the aluminum layer 20 and the refractory metal layer 18 is greater within the contact opening 16 due to its three-dimensional nature. Therefore, more aluminum/refractory metal alloy is formed within the contact opening 16. Since the alloy has a greater volume than the aluminum and refractory metal separately, the contact opening is filled to an extent which tends to level the upper surface of th aluminum layer 20. This provides for a relatively flat upper surface for aluminum layer 20, and this effect tends to improve the planarity of aluminum layer 20 to a greater degree as the width of contact opening 16 decreases. Thus, the present techniqu is especially suitable for use with contact openings having dimensions of less than one micron.

Figure 3 shows the aluminum/refractory metal alloy 22 as completely filling the contact opening 16. However, this is not always the case, as the aluminum layer 20 may extend into the opening 16. The alloy formed in the contact opening improves the planarity of the aluminum layer 20 even it it does not completely fill the opening 16.

Referring to Figure 4, an alternative embodiment of the present method is shown. After th contact opening 16 has been formed, a layer of refractory metal such as titanium is deposited and reacted as known in the art to form a layer of metal silicide 24. Following formation of the silicide layer 24, another thin layer 26 of refractory metal is deposited over the surface of the chip.

Several alternatives exist for formation of th refractory metal containing layer 24 and layer 26. As described in connection with Figure 2, a layer of refractory metal only, such as titanium or tungsten, can be used. A sandwich structure of refractory metal/refractory metal compound/refractory metal can be used, such as Ti/TiN/Ti. A sandwich of refractory metal silicide/refractory metal compound/refractory metal can also b used, such as $TiSi_X$/TiN/Ti. Th upper surface of th refractory metal-containing layer should hav enough refrac-

tory metal available to alloy with the aluminum.

Referring to Figure 5, an aluminum layer 28 is deposited ov r the chip at the elevated temperatures described above. This forms an aluminum/refractory metal layer 30 as before. Layer 26 is deposited over the chip because the silicided layer 24 does not have enough unalloyed refractory metal to combine with the aluminum layer 28 to the degree desired. Other layers of refractory metal compounds, such as titanium nitride, also preferably incorporate the deposition of an additional refractory metal layer 26 as described in Figures 4 and 5.

Since the alloying caused by the presently described technique results in a significant improvement in planarity of the aluminum layer of interconnect, it is possible to fabricate two or more contacts stacked one above the other. Such a stacked contact is shown in Figure 6.

After formation of aluminum layer 20 as described in connection with Figure 3, the interconnect layer is patterned as known in the art. A dielectric layer 32 is then formed over the surface of the chip and planarized. An opening 34 is formed in dielectric layer 32, followed by deposition of a refractory metal layer 36 over the surface of the chip. An aluminum layer 38 is deposited, as before, at an elevated temperature, causing formation of an aluminum/refractory metal alloy ,40. This forms a second level of metal interconnect, which is then patterned to give the structure shown in Figure 6.

If desired, a third metal interconnect layer can be fabricated on top of the structure shown in Figure 6 using the techniques described above. Due to the planarization caused by the described technique, multiple interconnect levels are more easily fabricated than has been the case in the past. This allows for complex signal routing to be performed using metal interconnect layers, which becomes more and more desirable as device densities increase.

Since the contact openings become completely filled with an aluminum/refractory metal alloy, aluminum step coverage problems at such contact opening are virtually eliminated. The aluminum/refractory metal alloy is more resistant to electromigration, and overall current densities remain relatively low since the contact opening is completely filled.

Although the invention has been described with reference to a specific embodiment, this description is not meant to be construed in a limiting sense. Various modifications of the disclosed embodiment as well as alternative embodiments of the invention will becom apparent to persons skilled in the art upon reference to the description of the invention. It is therefore contemplated that the appended claims will cover any such modifications or embodiments that fall within the tru scope of the invention.

Claims

1. A method for fabricating interlevel contacts in integrated circuits, comprising the steps of:
   forming a contact opening in an insulating layer to expose a conducting region beneath;
   depositing a conducting layer containing a refractory metal over the insulating layer and in the contact opening; and
   depositing an aluminum layer at a temperature exceeding approximately 150°C, wherein an alloy of aluminum and the refractory metal is formed in the contact opening.

2. The method of Claim 1, wherein the aluminum layer is deposited at a temperature in the range of 350°C to 500°C.

3. The method of Claim 2, wherein the aluminum layer is deposited at a rate of approximately 20-200 A/sec.

4. The method of Claim 1, wherein the alloy formed in the contact opening has a volume greater than that of unalloyed aluminum and the refractory metal.

5. The method of Claim 1, wherein the conducting layer containing refractory metal comprises a refractory metal compound.

6. The method of Claim 1, wherein said deposition of a conformal layer containing refractory metal step comprises the steps of:
   forming a refractory metal layer over the insulating layer and within the contact opening;
   reacting the refractory metal layer to form a refractory metal compound; and
   forming a second refractory metal layer over the reacted compound layer.

7. The method of Claim 6, wherein said reacting step comprises reacting the refractory metal to form a refractory metal nitride.

8. The method of Claim 6, wherein said reacting step comprising reacting the refractory metal layer to form a refractory metal silicide.

9. The method of Claim 1, wherein the contact opening is formed over a previously fabricated contact to a lower level conducting structure.

10. A method for fabricating interlevel contacts in an integrated circuit, comprising the steps of:
forming an opening in an insulating layer to expose a conductive region beneath;
depositing a conducting layer containing refractory metal over the insulating layer and within the opening; and
depositing aluminum at a temperature sufficient to cause the aluminum to alloy with the refractory metal at an interface thereof.

11. The method of Claim 10, wherein said deposition of a conducting layer containing refractory metal step comprises the steps of:
forming a refractory metal layer over the insulating layer and within the contact opening;
reacting the refractory metal layer to form a refractory metal compound; and
forming a second refractory metal layer over the reacted compound layer.

12. The method of Claim 11, wherein said reacting step comprises reacting the refractory metal to form a refractory metal nitride.

13. The method of Claim 11, wherein said reacting step comprises reacting the refractory metal layer to form a refractory metal silicide.

14. A semiconductor structure comprising:
an insulating layer overlying a conductive region;
an opening formed in said insulating layer and exposing a portion of the conducting region;
a layer containing refractory metal overlying said insulating layer, and covering sidewalls of the opening and the exposed portion of the conducting region;
a layer containing an alloy of aluminum and the refractory metal overlying said layer containing refractory metal; and
a layer of aluminum overlying said alloy containing layer.

15. The semiconductor structure of Claim 14, wherein said layer containing refractory metal comprises:
a layer of refractory metal silicide; and
a layer of refractory metal overlying said metal silicide layer.

16. The semiconductor structure of Claim 14, wherein said layer containing refractory metal comprises:
a layer of refractory metal nitride; and
a layer of refractory metal overlying said metal nitride layer.

17. A semiconductor structure according to Claim 14, further comprising:
a second insulating layer covering said aluminum layer and said first insulating lay r;
a second opening in said second insulating layer, wherein said second opening exposes a portion of said aluminum layer;
a second layer containing refractory metal overlying said second insulating layer, and covering sidewalls of said second opening and the exposed portion of said aluminum layer;
a second layer containing an alloy of aluminum and the refractory metal overlying said second layer containing refractory metal; and
a second layer of aluminum overlying said second alloy containing layer.

Fig.4.

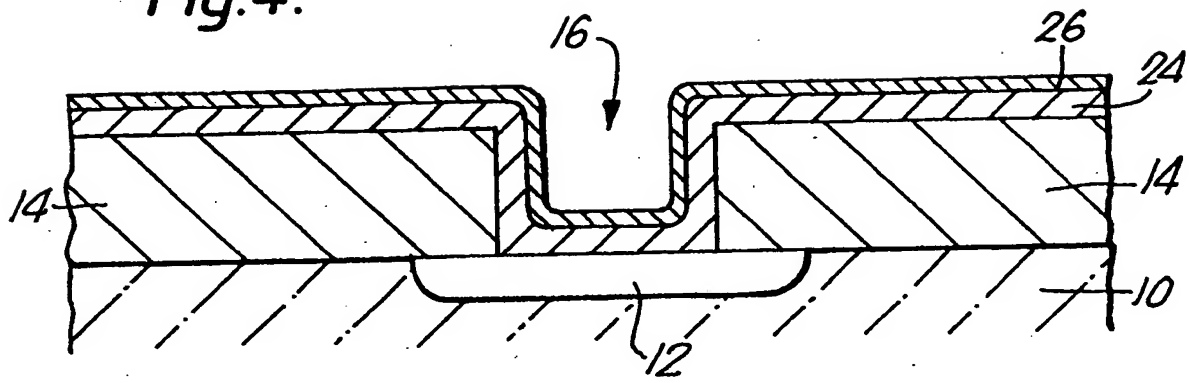

Fig.5.

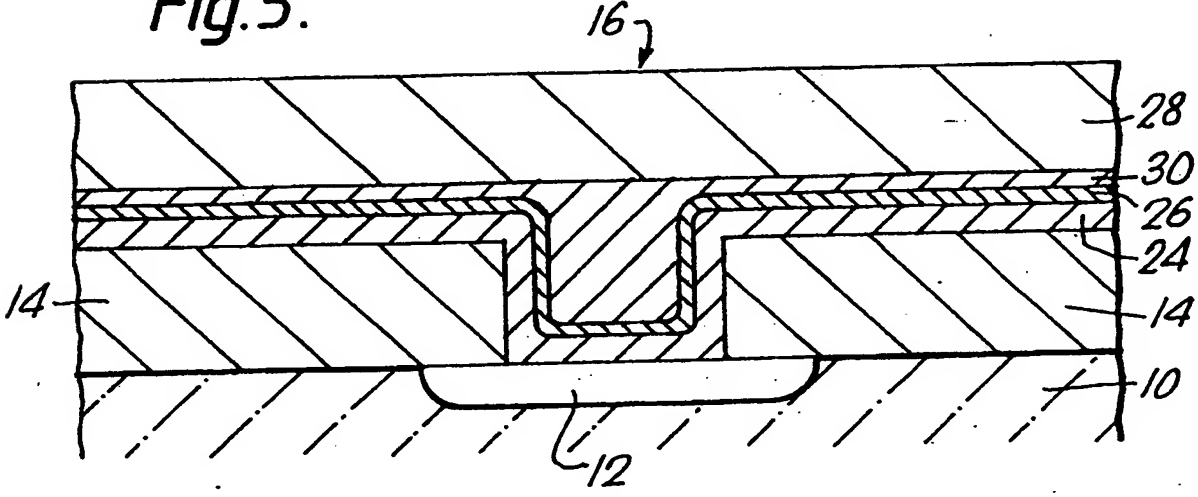

Fig.6.